

CSRP 572 – Low Overhead Self-Checking Combinational and Sequential Circuits Designed by Evolution

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Abstract

Evolutionary techniques are applied to the design of self-checking digital circuits in simulation. For the combinational and sequential benchmarks attempted, evolved designs are totally self-checking with respect to single stuck-at faults in mission logic, have no latency and use significantly less resources than hand-designed equivalents. The approach can be extended to evolve fail-safe circuits, analog self-test, and self-checking checkers under multiple faults.

1 Introduction

As hardware is increasingly used in mission critical applications such as medicine, transport, space and industry, avoiding faulty circuit behaviour can save lives and money. Permanent and transient hardware faults occurring in the field become of increasing concern as component density increases, costs are minimised in mass produced products, and hardware is deployed in more hostile environments. This paper demonstrates that artificial evolution can be used to design self-checking circuits superior to the best equivalents found in the literature for small benchmarks.

Off-line built-in self-test (BIST) techniques [31, 37, 10] are used to scan large circuits for faults post-manufacturing. Some circuits with on-line BIST using scan methods require the mission logic to go off-line temporarily or exhibit fault latency [28, 3]. *Self-checking* (SC) circuits perform concurrent error detection during normal operation, are necessary for detecting transient faults and are desirable in mission critical applications where mission hardware must neither stop nor fail without warning. *Self-testing* [30] circuits containing a fault will have a non-codeword at the outputs for some input codeword. *Fault-secure* circuits containing a fault will under all input codewords either be unaffected or output a non-codeword. *Totally Self-Checking* (TSC)

circuits are self-testing and fault-secure. Sequential TSC circuits must also produce non-codeword outputs for false state transitions. The most stringent SC designs are TSC checkers which under multiple faults to mission and testing logic satisfy the following: “*the first erroneous output resulting from an internal fault of the digital circuit is detectable.*”

Traditional SC architecture involves duplicating mission logic – sometimes with diversity [2] or inversion with two-rail logic – and comparing the duplicated outputs, thus achieving full fault-coverage of mission logic. Error detecting codes (EDC) such as Hamming, parity [26], 1-of-n [11] and Berger [24] can achieve lower overhead often at the expense of fault coverage. Berger codes are used in self-checking checkers detecting multiple unidirectional faults under certain assumptions. SC Synchronous Sequential Circuit (SSC) design methods have several limitations [27] yet sometimes achieve error recovery under transient faults [19] and there have been cases of less than duplication overhead [5] with near full fault coverage. It is generally accepted [11] to [11] aulss]been][5]fe89D[Tusa-(and)-228.9(there)-2dom

egy. A TSC edge-triggered D-latch (ETDL) was also evolved equivalent to D&C. This previous work has es-

SIS [4] using the script recommended in the manual for Xilinx LUT architectures. In order to save time and given that evolution is able to modify hand-designed circuits [8, 36] every run was seeded with the synthesised design of the mission logic. In the runs referred to as *Locked* the mission logic is immutable and evolution must find ways of performing SC without modifying it.

Even when evolving combinational circuits the evolving networks may be recurrent and could show an unwanted dependence on the order in which inputs are presented, and on the networks' internal state. To demand insensitivity to input ordering, the same approach was taken as for the randomization of logic delays (above): at the start of each generation, e (the same number e defining the number of evaluations with random gate delays above) different orderings of the full set of possible inputs for that task were generated, and the individuals of that generation evaluated on all of them. On each of the e evaluations the circuit state was reset, then the ordering of the full set of inputs was presented twice in sequence, to prevent dependence on initial conditions.

The same procedure was carried out for the sequential task excepting the random test pattern generation: a directed graph built from the Moore FSM of the benchmark circuit is built such that some nodes are assigned as reset states and enough edges are marked as permanent so that all states can be reached by moving along them. We first choose a reset state to start from and add the input pattern necessary to bring the FSM to this state from any other onto the generated test pattern. A random walk is now begun such that walking along an edge appends its input vector to the generated pattern and removes it from the graph unless it is marked permanent. The walk ends when all edges have been walked along thus ensuring that the random test pattern generated will test all FSM state transitions.

The task evaluation score was measured as follows. Let Q_r be the series of values at the r^{th} output bit for the final 15 time-slices of the presentation of each input, concatenated over all input vectors presented during an evaluation, and Q'_r the desired response. We take the modulus of the correlation of Q_r and Q'_r , averaged over all N outputs:

$$f_t = \frac{\sum_{r=0}^{N-1} |\text{corr}(Q_r, Q'_r)|}{N} \quad (1)$$

2.4 Evolving Self-Checking

An extra output E was recorded from circuits with the aim that it would go high whenever a fault affected any other output. The performance of a circuit at its main task f_t and at SC behaviour f_c were evaluated separately. SC behaviour was evaluated with three fitness measures:

1. Per fault f_{c_F} : Let u_f be the number of faults affecting task performance for which none of the possible input vectors raises E . Then f_{c_F} encourages faults to be 'detectable': $f_{c_F} = 1 / (1 + u_f \times k_f)$ where k_f was chosen to be 25, to give f_{c_F} good sensitivity when u_f is small.
2. Per instance f_{c_I} : Let SFI denote a combination of circuit state, SSA fault, and input vector. Define u_i to be the number of instances out of all possible SFI combinations for which the task output is incorrect but E is low. Then f_{c_I} encourages immediate detection of faults: $f_{c_I} = 1 / (1 + u_i \times k_i)$ where k_i was chosen to be 200.
3. Per transition f_{c_T} : Let u_t be the number of SFI instances for which mission outputs are unaffected, E is low, but the transition to the next state is incorrect. f_{c_T} discourages FSM failure: $f_{c_T} = 1 / (1 + u_t \times k_t)$ where k_t was chosen to be 50.

f_{c_F} and f_{c_I} were used when evolving SC combinational benchmarks. If we define output codewords to have E low then f_{c_F} measures self-testing and f_{c_I} also measures fault-security, so a circuit with $f_{c_F} = f_{c_I} = 1$ is TSC. f_{c_I} and f_{c_T} were used for sequential benchmarks and $f_{c_I} = f_{c_T} = 1$ is required for TSC.

u_f is measured by evaluating task fitness f_t separately under all SSA faults to every unit able to affect the task outputs. The same set of e evaluation conditions chosen for the current generation is used. If f_t falls by at least 0.01 due to a fault, then it is considered to affect task performance. u_i is measured by comparing the output of the circuit at each SFI combination with its output for the same state and input under no faults. Outputs are deemed unaffected if they are not different for more than 5 time steps of the 15 over which they are monitored. To test sequential circuits at particular states they are run fault-free with the randomly generated test pattern and a circuit state snapshot is saved as they enter each state for the first time. At each state, for each fault,

circuit exhibiting a high E when no faults were in place was deemed to have $f_{c_F} = f_{c_I} = f_{c_T} = 0$.

It seems foolish to concentrate on the detection of faults at every instance when dealing with a circuit in which some faults are not detected at any instance. Fitness objectives were given hierarchical priorities. For combinational benchmarks the priorities in descending order were f_t, f_{c_F}, f_{c_I} while for sequential benchmarks they were f_t, f_{c_I}, f_{c_T} . When sorting the individuals for rank selection the comparison operator only considered an objective if higher priority objectives were equal. An extra objective encouraging parsimony was also used, having the lowest priority of all.

3 Results

The maximum number of logic units available to evolution was constrained between 30 and 110 (the genotype length consequently ranged from 300 to 2200 bits) and the time evolution was allowed to run varied from several hours to several weeks. These factors depended monotonically on the size of the benchmark. These runs were performed by the concerted effort of approximately 200 2GHz computers contributed by volunteers around the world [6].

SC circuits with full fault coverage and no error latency over SSA faults in mission logic were evolved for all benchmarks attempted. They all satisfy the TSC condition since during their operation E goes high before or immediately after outputs are incorrect due to a fault. All evolved results can be viewed and tested on-line in a visual digital logic simulator [6].

Table 1 compares the overhead of evolved self-checkers with equivalents produced by other means reported in the literature. On average, evolved TSC circuits require only 66.9% overhead over mission logic. This is an average 42.0% of the duplicate & compare (D&C) overhead. This is significantly lower than the average 73.2% of D&C overhead required by the best previous results out of [24, 11, 5] for this test suite.

We will now look at three evolved TSC circuits: HENMANIAC performs the b1 combinational benchmark, SMILODON and Oryx perform the mc sequential benchmark. By error at U_n we mean that unit n is behaving differently from how it would if there were no faults in the circuit. For example there is no error at $U = a + b$ if it is SSA 1 and $a = 1$, but there would be if $a = b = 0$.

3.1 HENMANIAC

This TSC b1 benchmark circuit is composed of 9 gates and detects all SSA faults affecting mission behaviour with a maximum 3 gate delay latency. Even though the Xilinx LUT synthesis procedures recommended in SIS produced circuit with 23% D&C overhead, a circuit with 6 gates for the b1 benchmark, the evolved circuit in Fig. 1 requires only 5 gates for mission outputs.

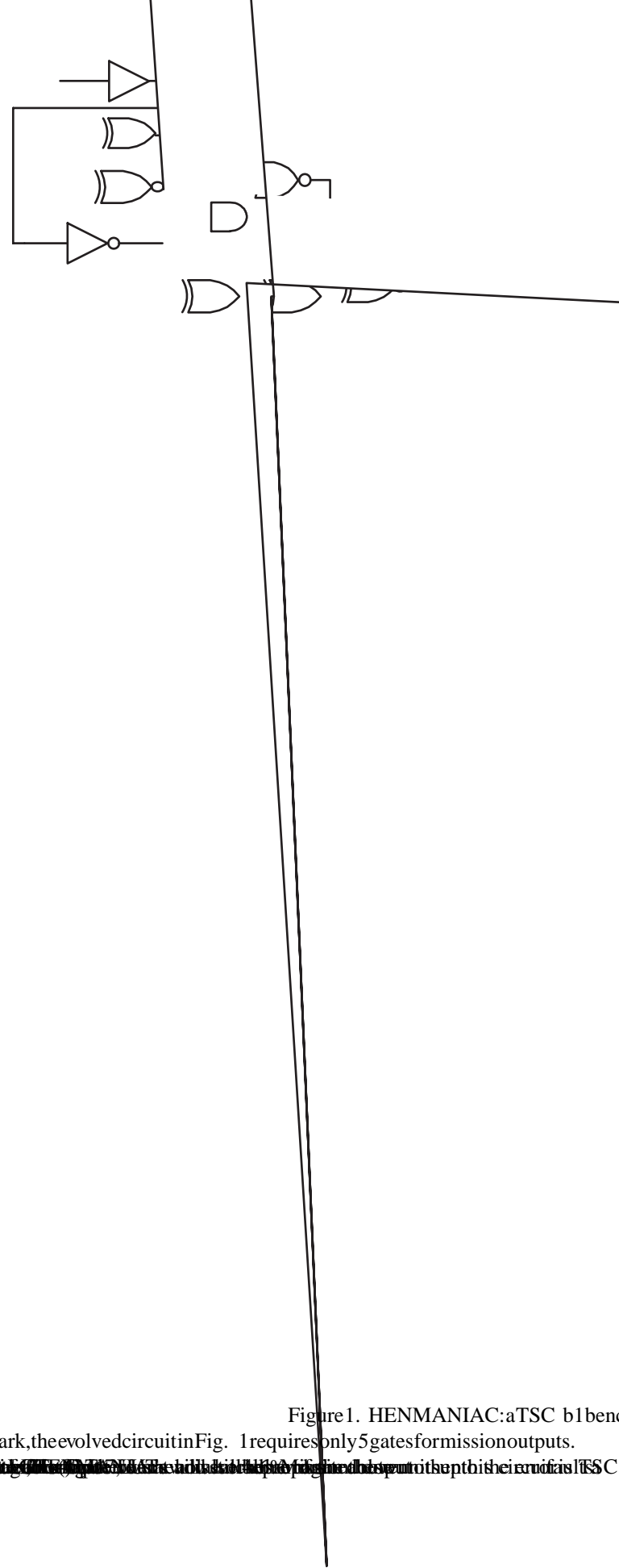


Figure 1. HENMANIAC: a TSC b1 benchmark circuit. The evolved circuit in Fig. 1 requires only 5 gates for mission outputs.

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whose sources U_9 and U_{14} are similar. Even though at first sight its operation seems to be using output cascading together with some recalculation as above (but with a non-modular structure similar to the multiplier in [7]), a more thorough investigation by observing dynamic circuit operation and analyzing LUT functions would provide more insight possibly uncovering novel useful principles of operation. However it is not the first time that efficient evolved circuits elude our understanding [35] due to evolution's capacity to exploit available resources fully without caring for modularity or other design principles. This circuit uses 15 units compared to 23 required for a D&C approach.

3.3 Oryx

This TSC circuit was not allowed to modify the 8 four-input LUTs and two latches generated by SIS for the mc benchmark. Two latches and 6 LUTs were added detecting all SSA faults in mission units. Some of these units are nearly duplicates of mission ones, others are fed the mission outputs together with circuit inputs. All 5 outputs are checked without modifying mission logic and with less than duplication (let alone comparison) overhead. It is possible that by such unconstrained evolution, an optimal EDC scheme has been found for this circuit.

3.4 Discussion

Even if LUT gate count is not an accurate measure of circuit area for every technology, this measure of overhead favours D&C as much as evolved circuits. For example the D&C overhead for the sequential benchmark dk27 is a copy of the optimised 8 units plus a single four-input LUT to compare both outputs. It would be possible to perform mapping onto a desired technology prior to parsimony fitness evaluation. It is believed that the power of evolution to exploit particular technologies would result in even greater overhead gains.

Some evolved SC circuits may have worse timing characteristics due to output cascading. However in many cases the amount of gate delays from inputs to outputs was not increased with respect to the original synthesised version. Moreover, circuit modifications are also required in order to make circuits unidirectional for use with Berger codes. Even then, the evolved TSC circuits with unmodified (locked) mission logic required an average 56.1% of D&C overhead still significantly lower than the previous best equivalent. The mission logic in these circuits has exactly the same specifications as before SC was added. This method could then be applied to specially designed circuits such as high speed or unmodifiable IP cores without disrupting their characteristics. If SC circuits with a certain characteristic were required, all that would be necessary would

be to add extra pressure in the fitness function. For example a fourth fitness measure selecting for circuits with low input-output delay could be added. In this way the nature of evolved circuits is highly customizable.

HENMANIAC can be trivially made into a self-checking checker under multiple faults under the assumption that *all input vectors are applied between faults arriving*. Replace U_4 so that E is taken from the output of one of two XOR gates connected back to back such that each of their outputs is an input of the other and the remaining inputs are taken from Y_2 and U_7 . Now define an error signal or non-codeword to be when E is non-oscillating. Now E will oscillate whenever $Y_2 \neq U_7$ and will stop otherwise. Since all SSA faults in all units except U_4 were detectable as soon as they caused errors at outputs, and SSA faults in the oscillating XORs will be detected immediately, then all SSA faults in all units are now detectable for some input vector and they never produce errors at any output without oscillation stopping. Thus this modified HENMANIAC is a totally self-checking checker under any amount of faults under the assumption above. After observation, various evolved TSC circuits operate in similar ways as HENMANIAC and could be modified to be self-checking checkers in a similar fashion.

Further analysis of SC mechanisms used by evolved circuits may arrive at mathematical models of EDC used. It is possible that such codes are tailored for each circuit by evolution finding the optimal one based on its characteristics.

Better results may have been found by evolution if given more time to run. It often took days of evolution to reduce the size of a circuit already fulfilling the TSC fitness criteria. These are not known to be optimal solutions since evolving for a few more days may have reduced the size even further.

lents found in the literature. In future as increasing amounts of processing power are available and the methodology matures, larger benchmarks should be within reach.

The principles of operation of evolved circuits are similar to those in [8, 7] such as cascading outputs, using non-canalizing functions and reusing units in a duplicated section such that errors at the units only affect the original or the duplicate. Even though the circuits analyzed share some of these, there may be uniquely tailored EDCs for each of them. The use of this method is two-fold. On the one hand TSC evolved circuits can themselves be used in mission critical applications. On the other, their analysis may provide understanding of their operation and this learning could be added to design techniques so that such low overhead TSC circuits could be synthesised without resorting to evolutionary search. This would not be the first time engineering has learnt from evolved designs such as those found in nature.

There are opportunities for extension of this work such as attempting larger benchmarks, other technology mappings, and including other circuit requirements such as timing. At the time of writing, self-testing checkers are being evolved detecting multiple faults assuming or not that all input vectors are applied between fault arrivals. TSC checkers without this assumption with full fault coverage and no latency are the ultimate goal of SC design and one such circuit has already been evolved. Future avenues also include evolution of SC analog hardware.

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